

REMARKS

Examiner Mitchell is thanked for the thorough examination and search of the subject Patent Application. Claims 21-23 have been amended.

All Claims are believed to be in condition for Allowance, and that is so requested.

Reconsideration of the rejection under 35 U.S.C. 103(a) of Claims 21-24, 26, 28, and 29 as being unpatentable over Sakurai et al in combination with Christiansen et al is requested in accordance with the following remarks.

The insulating film 14 of Sakurai et al is not the same as the epoxy layer 410 of Applicant's invention. Applicant's layer 410 is coated onto the substrate surface after formation of the copper pillars, as taught on page 10 of the Specification and as shown in the progression of drawing figures 4B-4D. Portions of the epoxy layer are then removed to expose the tops of the pillars. Solder balls are then formed covering the tops of the pillars. The insulating film 14 in Sakurai et al is formed to cover the pads 12 (paragraph [0097]). Openings are etched through the insulating film 14 to the pads 12. The conductive pillars 30 (Fig. 2) or 90 (Fig. 12) are formed within the openings in the film 14. That is, the insulating film 14 is formed prior to forming the pillars in Sakurai et al while the epoxy 410 in Applicant's invention is formed after forming the pillars.

Sakurai et al does not teach or suggest an epoxy layer covering a portion of the side surfaces of the conductor. Christiansen et al teaches that an epoxy glob can provide passivation “separately covering each chip” (col. 5, lines 2-4). This is done after “completion of wire bonding ... for the entire circuit board” (col. 4, lines 63-67). Thus, this epoxy glob does not cover a portion of the side surfaces of the conductor, but covers the entire chip. It is not agreed that this epoxy glob encapsulating entire chips has anything to do with the insulating layer of Sakurai et al. Sakurai et al form an insulating layer 14 covering pads on a chip [0097]. This layer is formed in the process of forming a bump on the pad. The term “epoxy glob” seems to indicate that a large amount of epoxy is dispensed to cover the entire chip. No etching away of the “epoxy glob” is performed. Sakurai’s insulating layer 14 could not be a large amount of epoxy or it would be difficult to etch openings to the pads through the layer 14. Thus, it is not agreed that there would be motivation to use the epoxy of Christiansen et al in the process of Sakurai et al.

Reconsideration of the rejection under 35 U.S.C. 103(a) of Claims 21-24, 26, 28, and 29 as being unpatentable over Sakurai et al in combination with Christiansen et al is requested in accordance with the remarks above.

Reconsideration of the rejection under 35 U.S.C. 103(a) of Claim 25 as being unpatentable over Sakurai et al and Christiansen et al and further in combination with Jin is requested in accordance with the following remarks.

As discussed above, it is not agreed that there would be any motivation to use the epoxy of Christiansen et al in place of the insulating layer of Sakurai et al. While it is agreed that Jin teaches nickel and gold layers 30 and 32 under reflowable material 36 (Fig. 12), the combination of Jin with Sakurai et al and Christiansen et al would not result in Applicant's invention since none of the references teach or suggest an epoxy layer covering a portion of the side surfaces of the conductor.

Reconsideration of the rejection under 35 U.S.C. 103(a) of Claim 25 as being unpatentable over Sakurai et al and Christiansen et al and further in combination with Jin is requested in accordance with the remarks above.

Reconsideration of the rejection under 35 U.S.C. 103(a) of Claims 21, 24, 28, and 29 as being unpatentable over Zuniga-Ortiz et al in combination with Test et al is requested in view of amended claims 21-23 and in accordance with the following remarks.

Claims 21-23 have been amended to claim "pillar conductors" as taught on page 8 of the Specification. Zuniga-Ortiz et al do not teach pillar conductors. As shown in Fig. 1, the conductor 105,106,107 is deposited conformally on the UBM layer 103 (paragraph [0031]). This is not a pillar conductor as taught in Applicant's invention and as now claimed in Claim 21.

Therefore, the combination of Zuniga-Ortiz et al with Test et al does not teach or suggest the epoxy layer covering a portion of the side surfaces of a pillar conductor and the reflowable

material covering another portion of the side surfaces of the pillar conductor not covered by the epoxy layer.

Reconsideration of the rejection under 35 U.S.C. 103(a) of Claims 21, 24, 28, and 29 as being unpatentable over Zuniga-Ortiz et al in combination with Test et al is requested in view of amended Claims 21-23 and in accordance with the remarks above.

Allowance of all Claims is requested.

It is requested that should Examiner Mitchell not find that the Claims are now Allowable that the Examiner call the undersigned at 845-452-5863 to overcome any problems preventing allowance.

Respectfully submitted,

A handwritten signature in black ink, appearing to be 'SBA', with a long horizontal flourish extending to the right.

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